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10/751,372	01/05/2004	Henry W. Koertzen	P17683	2216

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BUCKLEY, MASCHOFF, TALWALKAR LLC
5 ELM STREET
NEW CANAAN, CT 06840

EXAMINER

TRUJILLO, JAMES K

ART UNIT	PAPER NUMBER
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2116

DATE MAILED: 07/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/751,372	KOERTZEN ET AL.	
	Examiner	Art Unit	
	James K. Trujillo	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-38 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-38 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 January 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|----------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>010504</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The office acknowledges the receipt of the following and placed of record in the file:
Submission of Application dated 1/5/04.
2. Claims 1-38 are presented for examination.

Drawings

3. The drawings are objected to because the unlabeled rectangular box(es) shown in the drawings (figures 4 and 6) should be provided with descriptive text labels. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. Claims 3-7, 12-14, 18-20, 22, 25, 30-32, and 36-38 are objected to because of the following informalities:

- a. Regarding claim 3, on line 1, “supply voltage” should be preceded by an identifier such as “output” in order to distinguish it from the “first” and “second” supply voltage values in order to particularly point out and distinctly claim the subject matter. It is believed that the “supply voltage” is intended to be different from the “first” and “second” supply voltage values and for examination purposes it will be interpreted as such.
- b. Regarding claims 4-7, they are dependent upon claim three and therefore suffer the same problems.
- c. Further regarding claims 4, 5 and 7, these claims also recite “supply voltage” and should be corrected in a similar manner as for claim 3.
- d. Further regarding claim 7, it also recites “a supply current” should be preceded by an identifier such as “output” in order to distinguish it from the “first” and “second” supply current values in order to particularly point out and distinctly claim the subject matter.
- e. Regarding claims 12-14, 18-20, 22, 25, 30-32, and 36-38, they have similar problems as those in claims 3-7.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

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5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

6. Claims 1-4, 7-14, 9-14, 16-32 are rejected under 35 U.S.C. 102(a) as being anticipated by Horigan et al., U.S. Patent 6,566,848.

7. Regarding claim 1, Horigan teaches an apparatus comprising: a first device (voltage regulator 20) to receive (the voltage regulator adjusts and recalibrates the load line based on the associated points therefore the voltage regulator receives the signals, col. 4, lines 17-19) a first signal representing a first supply voltage value associated with a first supply current value (point A on load line 19 in figure 3, col. 3, lines 5-15), and representing a second supply voltage value associated with a second supply current value (point C on load line 19 in figure 3, col. 3, lines 26-30).

8. Regarding claim 2, Horigan taught the apparatus according to claim 1, as described above. Horigan further teaches wherein the first signal represents an impedance value (the first signal of Horigan represents a load line which inherent represents an impedance value as its slope, figures 1 and 3).

9. Regarding claim 3, Horigan taught the apparatus according to claim 1, as described above. Horigan further teaches the first device to adjust an *output* supply voltage to a value based at least in part on the first signal (the voltage regulator of Horigan supplies Vcc according to the load line, col. 2, lines 32-37 and figures 1 and 3).

10. Regarding claim 4, Horigan taught the apparatus according to claim 3, as described above. Horigan further teaches the first device comprising: a voltage regulator converter to generate the *output* supply voltage (a converter is inherent in Horigan in order for regulator 20 to produce an output voltage); and a voltage regulator converter to receive the first signal and to transmit a control signal to the voltage regulator converter, the control signal to control the value of the supply voltage (points representing voltages and current are measured and the regulator uses them to establish a load line, therefore the measurements must be sent to the voltage regulator, col. 3, lines 5-30).

11. Regarding claim 7, Horigan taught the apparatus according to claim 1, as described above. Horigan further teaches wherein the supply voltage is associated with a supply current, wherein the first supply voltage value and the first supply current value define a first coordinate of a voltage vs. current coordinate system (point A, figures 1 and 3), wherein the second supply voltage value and the second supply current value define a second coordinate of the voltage vs. current coordinate system (point C, figures 1 and 3), wherein the first coordinate and the second coordinate define a line (load lines 19 and 41, figures 1 and 3 respectively), wherein the value of the supply voltage and a value of the supply current define a third coordinate (an operating point of the voltage regulator along the load line), and wherein the line substantially comprises the third coordinate (an operating point along a load line inherently comprises a third coordinate).

12. Regarding claim 8, Horigan taught the apparatus according to claim 1, as described above. Horigan further teaches wherein the first signal represents a slope of a power supply load line (points A and C represent a slope of a power supply load line, figures 1 and 3).

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13. Regarding claims 9-14, 16-21, and 27-32, Horigan taught claimed apparatus for receiving a first signal therefore he also teaches the claimed methods for receiving and transmitting a first signal and the claimed apparatus for transmitting the first signal.

14. Regarding claim 22, Horigan taught the apparatus according to claim 16, as described above. Horigan taught further comprising: adjusting a supply voltage having a value based at least in part on the first signal (adjusting the voltage along load line 19 or 41, figures 1 and 3 respectively); and receiving a second signal representing a third supply voltage value associated with the first supply current value, and representing a fourth supply voltage value associated with the second supply current value (points D and B on load lines 18 and 40, figures 1 and 3).

15. Regarding claim 23, Horigan taught the apparatus according to claim 22, as described above. Horigan further teaches wherein the second signal represents a second impedance value (load lines 18 and 40 inherently represent a second impedance value, figures 1 and 3).

16. Regarding claim 24, Horigan taught the apparatus according to claim 22, as described above. Horigan further teaches wherein the second signal represents a slope of a second power supply load line (load lines 18 and 40 represent a slope of a second power supply load line).

17. Regarding claim 25, Horigan taught the apparatus according to claim 22, as described above. Horigan further teaches further comprising: adjusting the supply voltage to a second value based at least in part on the second signal (supplying voltage from the voltage regulator according to load lines 18 or 40, figures 1 and 3).

18. Regarding claim 26, Horigan taught the apparatus according to claim 25, as described above. Horigan taught wherein the second supply voltage is associated with a second supply current, wherein the third supply voltage value and the first supply current value define a first

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coordinate of a voltage vs. current coordinate system, wherein the fourth supply voltage value and the second supply current value define a second coordinate of the voltage vs. current coordinate system, wherein the first coordinate and the second coordinate define a line, wherein the value of the second supply voltage and a value of the second supply current define a third coordinate, and wherein the line substantially comprises the third coordinate (end points D and B and operating point at which the voltage regulator supplies the output voltage, figures 1 and 3).

19. Claims 1-32 are rejected under 35 U.S.C. 102(a) as being anticipated by Hsu et al., U.S. Patent Application Publication 2004/0003310.

20. Regarding claim 1, Hsu teaches an apparatus comprising: a first device (voltage regulator 150) to receive (paragraph [0013]) a first signal representing a first supply voltage value associated with a first supply current value, and representing a second supply voltage value associated with a second supply current value (in order to determine a load line the signal would have to represent a first voltage associated with a first current and a second voltage associated with a second current, paragraph [0013]).

21. Regarding claim 2, Hsu taught the apparatus according to claim 1, as described above. Hsu further teaches wherein the first signal represents an impedance value (the first signal of Hsu represents a load line which inherent represents an impedance value as its slope, figures 1 and 3).

22. Regarding claim 3, Hsu taught the apparatus according to claim 1, as described above. Hsu further teaches the first device to adjust an *output* supply voltage to a value based at least in part on the first signal (the voltage regulator of Hsu supplies Vcc according to the load line, paragraph [0004]).

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23. Regarding claim 4, Hsu taught the apparatus according to claim 3, as described above.

Hsu further teaches the first device comprising: a voltage regulator converter to generate the *output* supply voltage (controller/driver 211, figure 2); and a voltage regulator converter to receive the first signal and to transmit a control signal to the voltage regulator converter, the control signal to control the value of the supply voltage (controller/driver 211, figure 2).

24. Regarding claim 5, Hsu taught the apparatus according to claim 3, as described above.

Hsu further teaches a second device to transmit the first signal and to receive the supply voltage (microprocessor provides the signal, paragraph [0013]).

25. Regarding claim 6, Hsu taught the apparatus according to claim 5, as described above.

Hsu further teaches wherein the second device comprises an integrated circuit (processor paragraph [0013]).

26. Regarding claim 7, Hsu taught the apparatus according to claim 1, as described above.

Hsu further teaches wherein the supply voltage is associated with a supply current, wherein the first supply voltage value and the first supply current value define a first coordinate of a voltage vs. current coordinate system (signal of Hsu defines load line 302 having a first coordinate, figure 3), wherein the second supply voltage value and the second supply current value define a second coordinate of the voltage vs. current coordinate system (signal of Hsu load line 302 having a second coordinate, figure 3), wherein the first coordinate and the second coordinate define a line (load line 302, figures 3), wherein the value of the supply voltage and a value of the supply current define a third coordinate (an operating point of the voltage regulator along the load line), and wherein the line substantially comprises the third coordinate (an operating point along a load line inherently comprises a third coordinate).

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27. Regarding claim 8, Hsu taught the apparatus according to claim 1, as described above.

Hsu further teaches wherein the first signal represents a slope of a power supply load line (load line 302 inherently has a slope, figures 3).

28. Regarding claims 9-14, 16-21, and 27-32, Hsu taught claimed apparatus for receiving a first signal therefore he also teaches the claimed methods for receiving and transmitting a first signal and the claimed apparatus for transmitting the first signal.

29. Regarding claim 22, Hsu taught the apparatus according to claim 16, as described above. Hsu taught further comprising: adjusting a supply voltage having a value based at least in part on the first signal (adjusting the voltage along load line 302, figures 3); and receiving a second signal representing a third supply voltage value associated with the first supply current value, and representing a fourth supply voltage value associated with the second supply current value (another signal representing load line 301, figures 3).

30. Regarding claim 23, Hsu taught the apparatus according to claim 22, as described above. Hsu further teaches wherein the second signal represents a second impedance value (load line 301 inherently represent a second impedance value, figures 3).

31. Regarding claim 24, Hsu taught the apparatus according to claim 22, as described above. Hsu further teaches wherein the second signal represents a slope of a second power supply load line (load line 301 represent a slope of a second power supply load line).

32. Regarding claim 25, Hsu taught the apparatus according to claim 22, as described above. Hsu further teaches further comprising: adjusting the supply voltage to a second value based at least in part on the second signal (supplying voltage from the voltage regulator according to load lines 310, figures 3).

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33. Regarding claim 26, wherein the second supply voltage is associated with a second supply current, wherein the third supply voltage value and the first supply current value define a first coordinate of a voltage vs. current coordinate system, wherein the fourth supply voltage value and the second supply current value define a second coordinate of the voltage vs. current coordinate system, wherein the first coordinate and the second coordinate define a line, wherein the value of the second supply voltage and a value of the second supply current define a third coordinate, and wherein the line substantially comprises the third coordinate (load lines 302 defines is a second load line, figures 3).

Claim Rejections - 35 USC § 103

34. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

35. Claims 33-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al., U.S. Patent Application Publication 2004/0003310 in view of Microsoft Computer Dictionary (Microsoft).

36. Regarding claim 33, Hsu teaches a system comprising:

- a. a microprocessor to transmit a first signal representing a first supply voltage value associated with a first supply current value, and representing a second supply voltage value associated with a second supply current value (the processor provides signals

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indicating amount of current under an operating condition, paragraphs [0013] and [0017]);

- b. a voltage regulator to receive the first signal (VR 150 figure 1); and
- c. a memory electrically coupled to the microprocessor (Main Memory 115, figure 115).

Hsu does not explicitly disclose wherein the memory is a double data rate memory.

Microsoft teaches a double data rate memory provides the advantage of doubling memory throughput (under definition of DDR SDRAM).

It would have been obvious to one of ordinary skill in the art, having the teachings of Hsu and Microsoft before them at the time the invention was made to modify the memory of Hsu to use the DDR SDRAM as taught by Microsoft.

One of ordinary skill in the art would have been motivated to make this modification in order to obtain the advantage of doubling memory throughput in view of the teachings of Microsoft.

37. Regarding claim 34, Hsu together with Microsoft taught the system according to claim 33, as described above. Hsu further teaches wherein the first signal represents an impedance value (the current will determine the impedance value for a given regulator output voltage, paragraph [0017]).

38. Regarding claim 35, Hsu together with Microsoft taught the system according to claim 33, as described above. Hsu further teaches wherein the first signal represents a slope of power supply load line (the voltage regulator determines a load line based on the signal, therefore it represents the slope of a load line, paragraph [0013]).

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39. Regarding claim 36, Hsu together with Microsoft taught the system according to claim 33, as described above. Hsu further teaches wherein the voltage regulator to adjust a supply voltage to a value based at least in part on the first signal (voltage regulator will supply voltage according to a load line, paragraph [0013]).

40. Regarding claim 37, Hsu together with Microsoft taught the system according to claim 33, as described above. Hsu further teaches the voltage regulator comprising:

- a. a voltage regulator converter to generate the supply voltage (controller/driver 211, figure 2); and
- b. a voltage regulator controller to receive the first signal and to transmit a control signal to the voltage regulator converter, the control signal to control the value of the supply voltage (controller/driver 211, figure 2).

41. Regarding claim 38, Hsu together with Microsoft taught the system according to claim 33, as described above. Hsu further teaches wherein the supply voltage is associated with a supply current, wherein the first supply voltage value and the first supply current value define a first coordinate of a voltage vs. current coordinate system, wherein the second supply voltage value and the second supply current value define a second coordinate of the voltage vs. current coordinate system, wherein the first coordinate and the second coordinate define a line, wherein the value of the supply voltage and a value of the supply current define a third coordinate, and wherein the line substantially comprises the third coordinate (paragraph [0033] and 420 of figure 4).

Conclusion

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42. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat. No. 6,919,715 to Muratov et al. teaches a system that alters a load line to adjust voltage droop.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (571) 272-3677. The examiner can normally be reached on M-F (8:00 am - 5:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



James K. Trujillo
Patent Examiner
Technology Center 2100